

Fig. 1

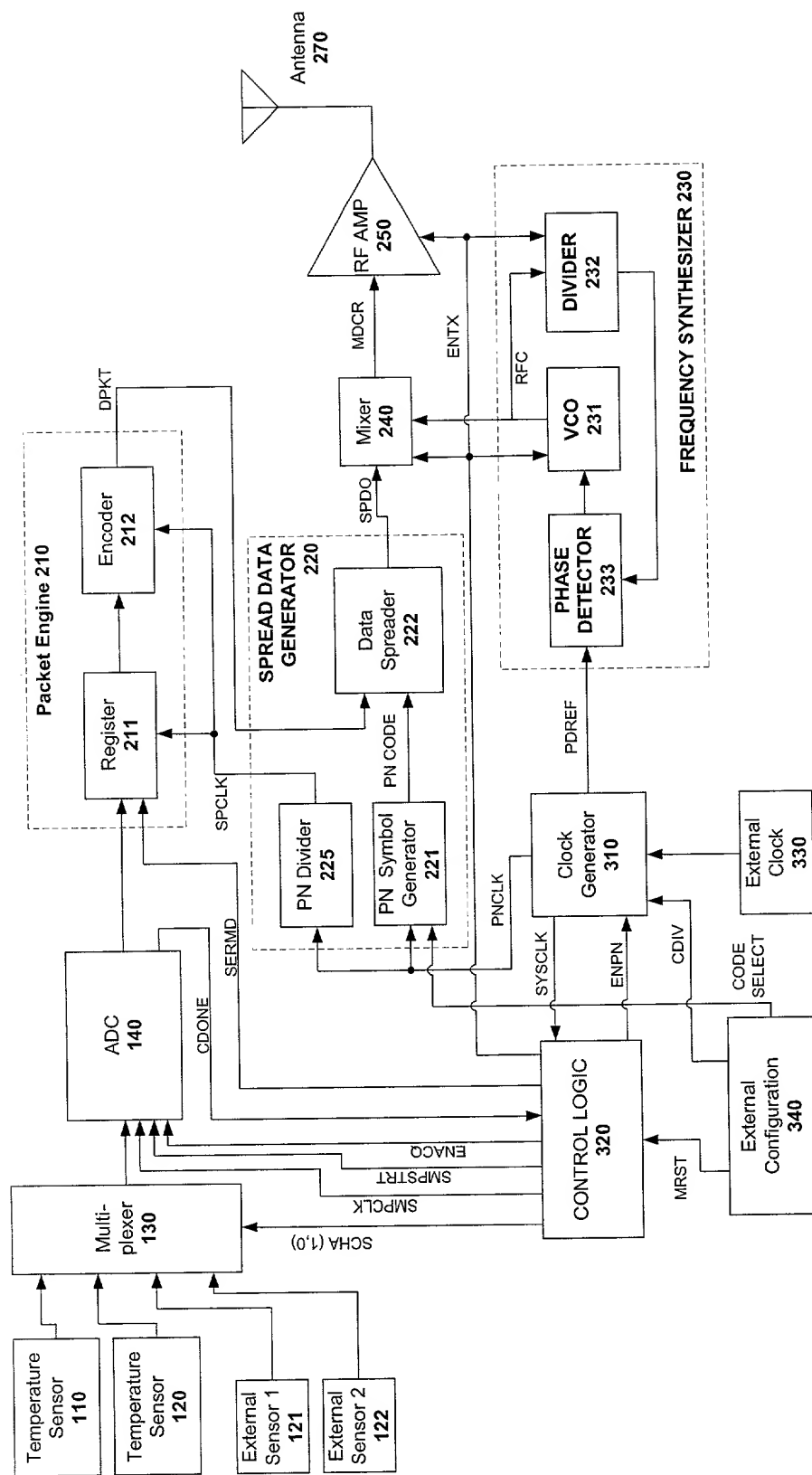
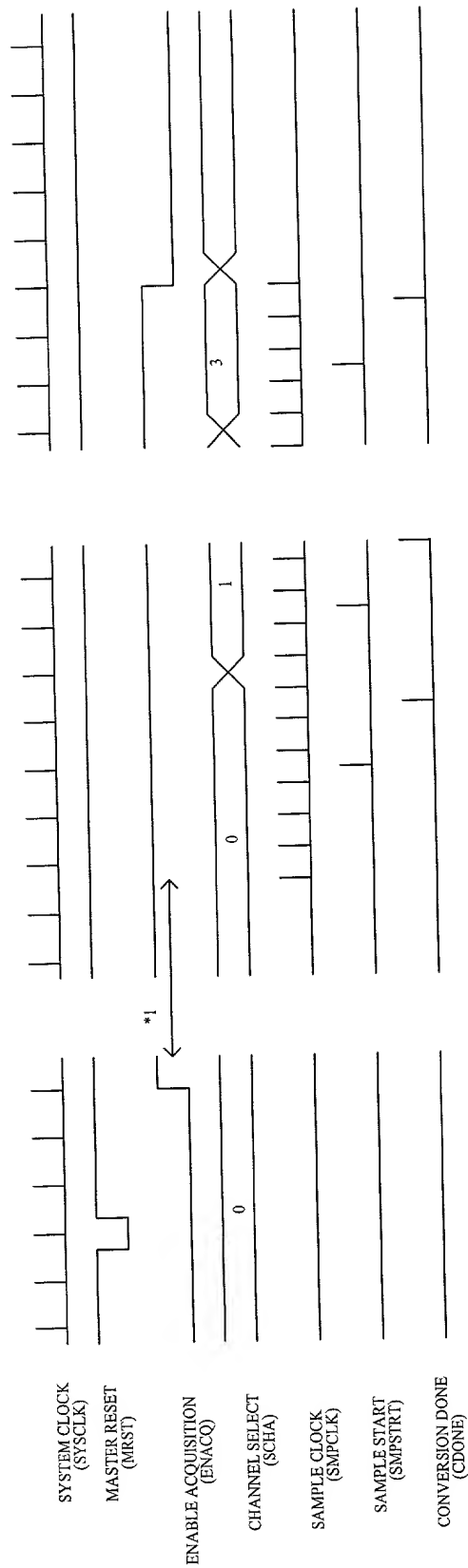


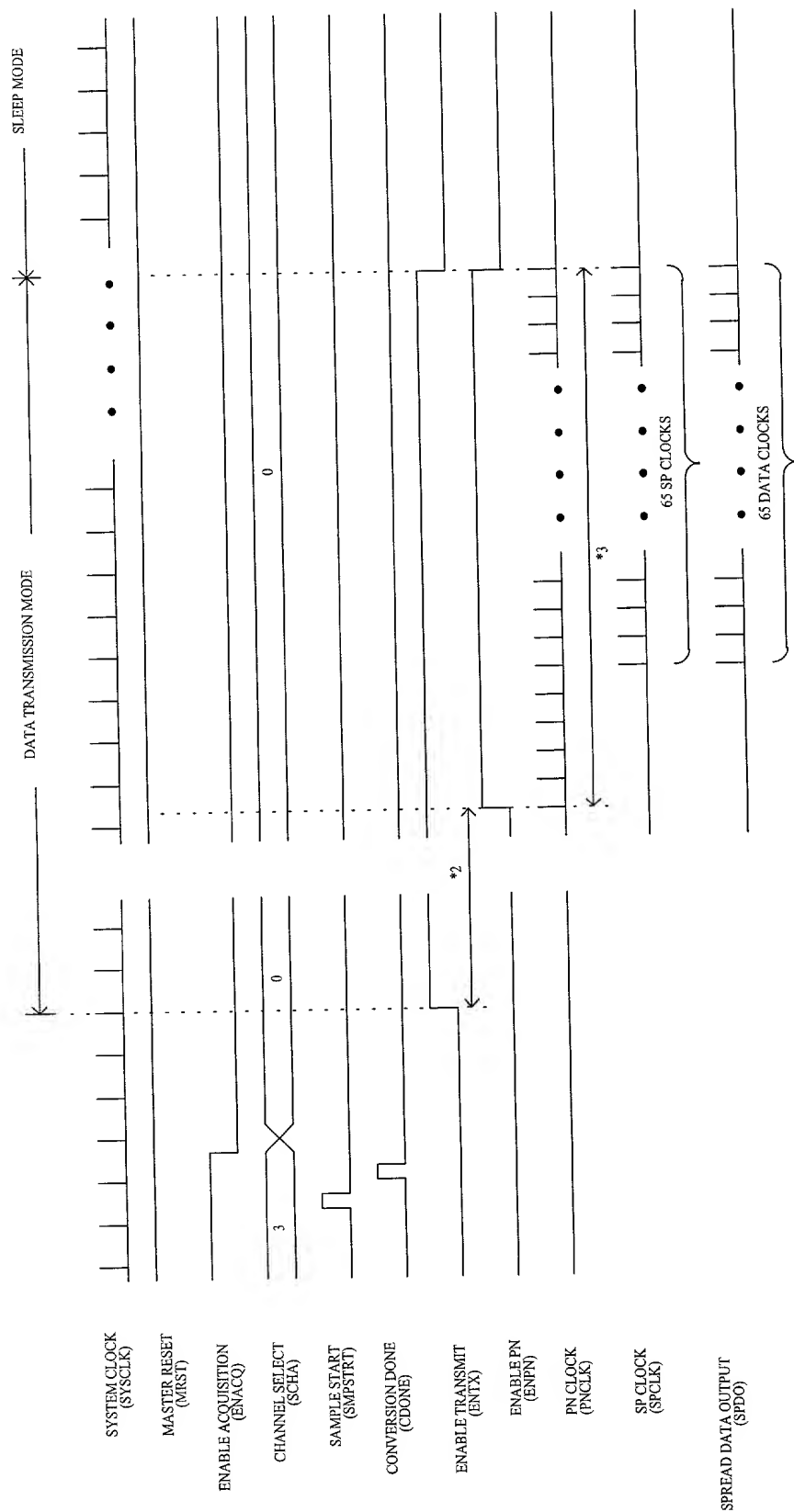
Fig. 2

DATA ACQUISITION CYCLE



*1 There are 1024 system clock cycles between enable acquisition and the beginning of the sample clock. This wait period is for acquisition component stability.

Fig. 3



*2 There are 1024 system clock cycles between enable transmit and the beginning of the transmit (PN) clock. This wait period is for transmit component stability.

*3 The SP clock is the PN clock divided by 53.

Fig. 4

ORNL TELESensor ASIC SYSTEM TIMING

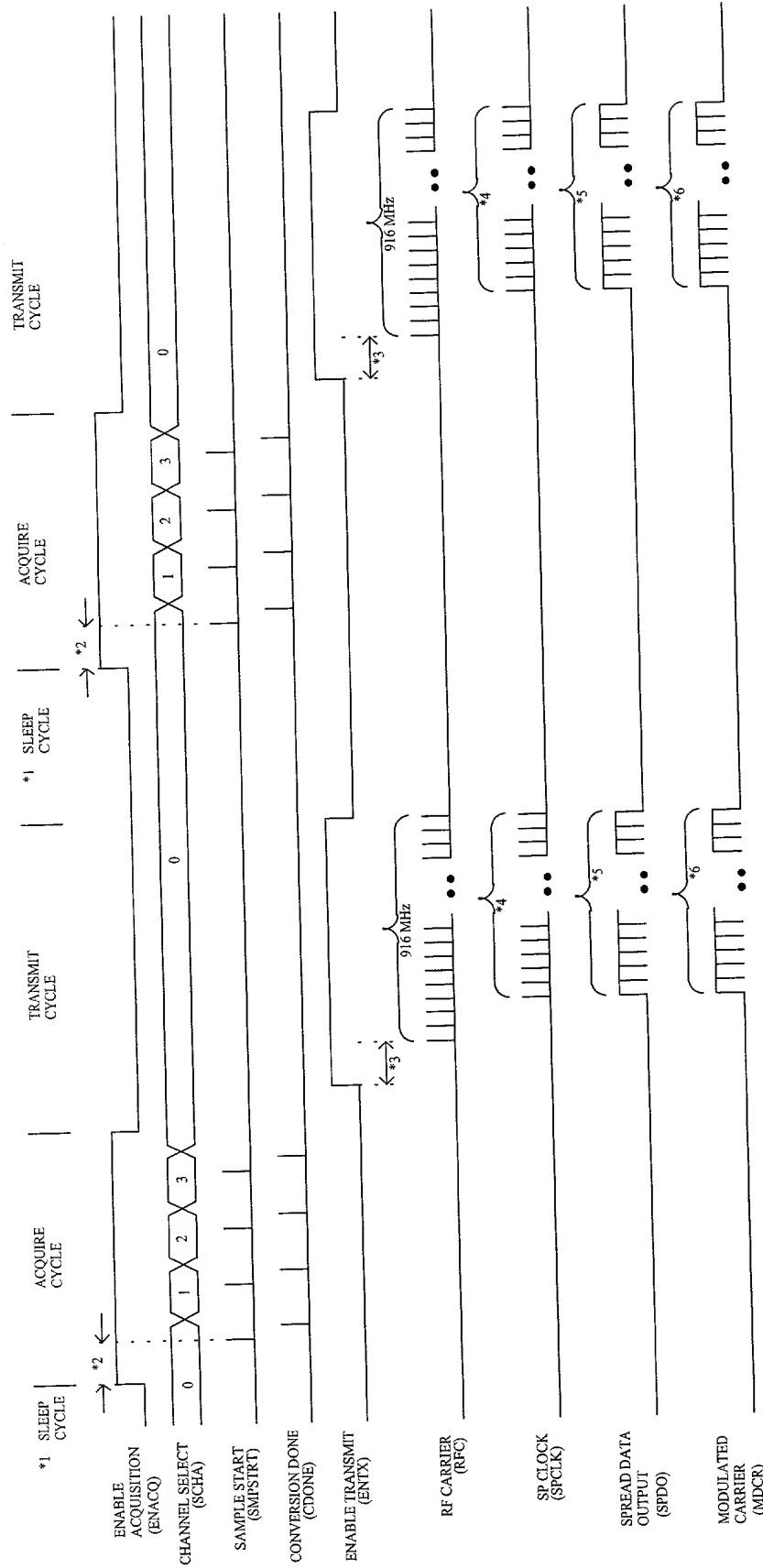


Fig. 5

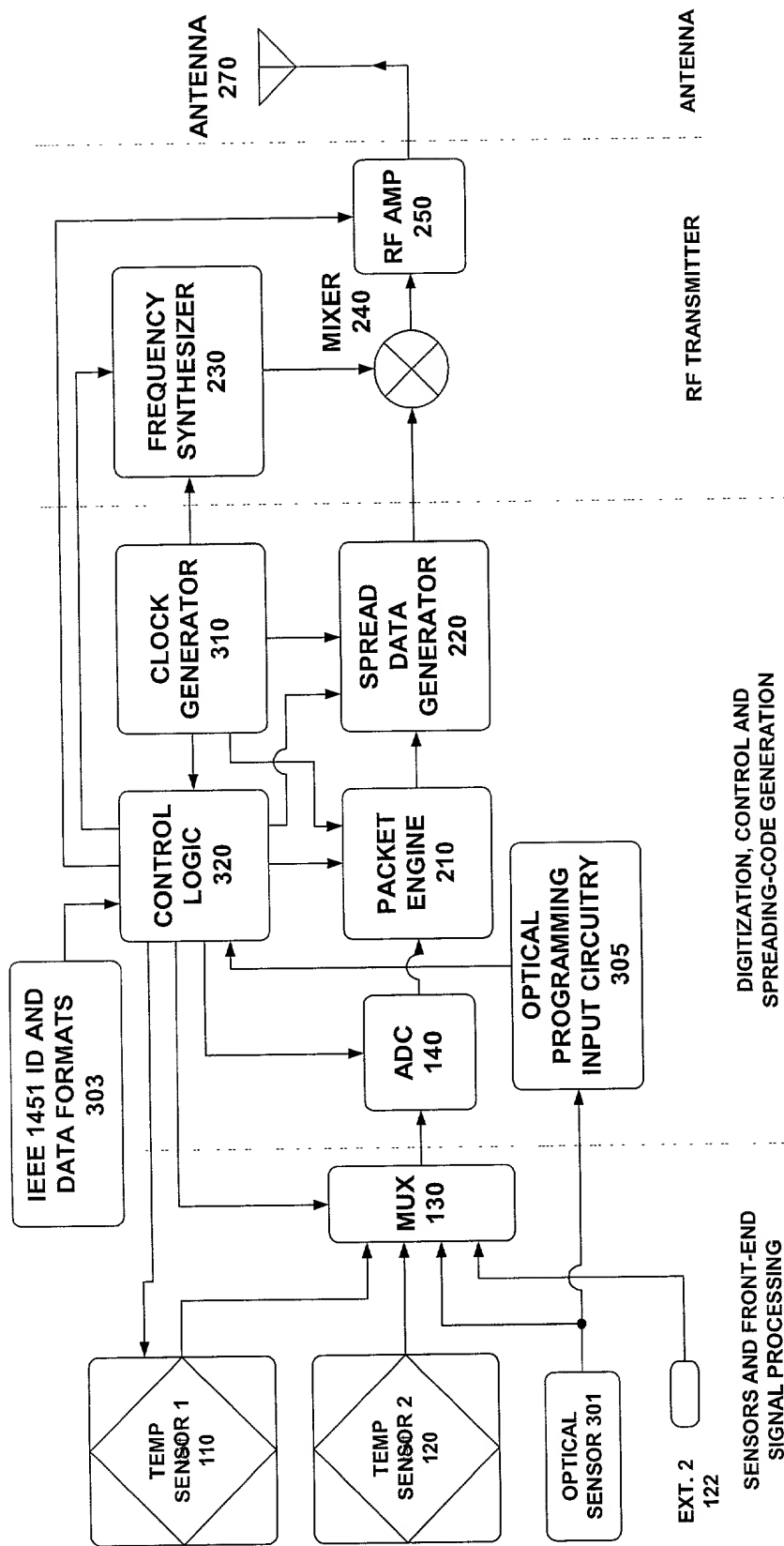


Fig. 6

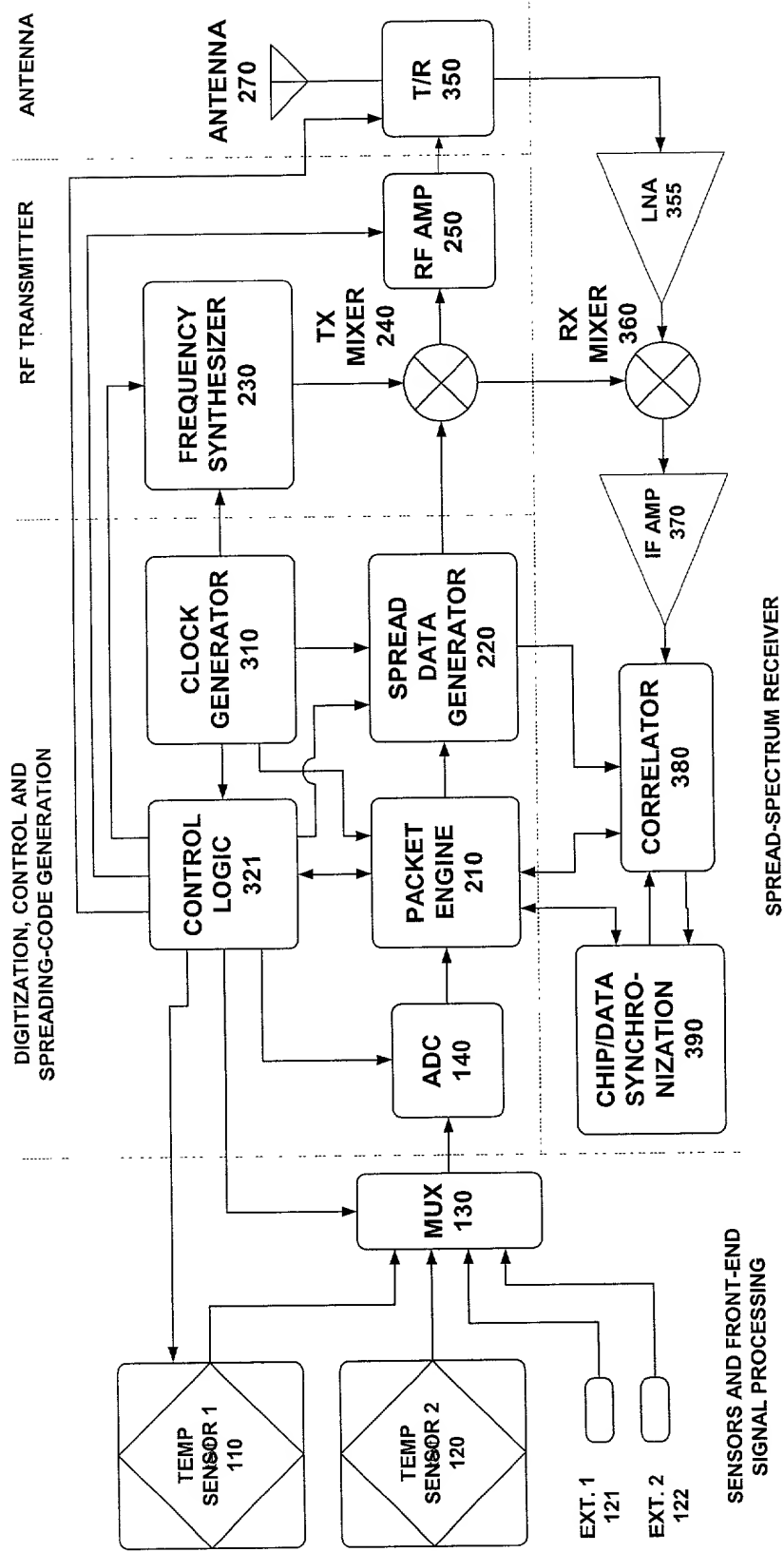


Fig. 7

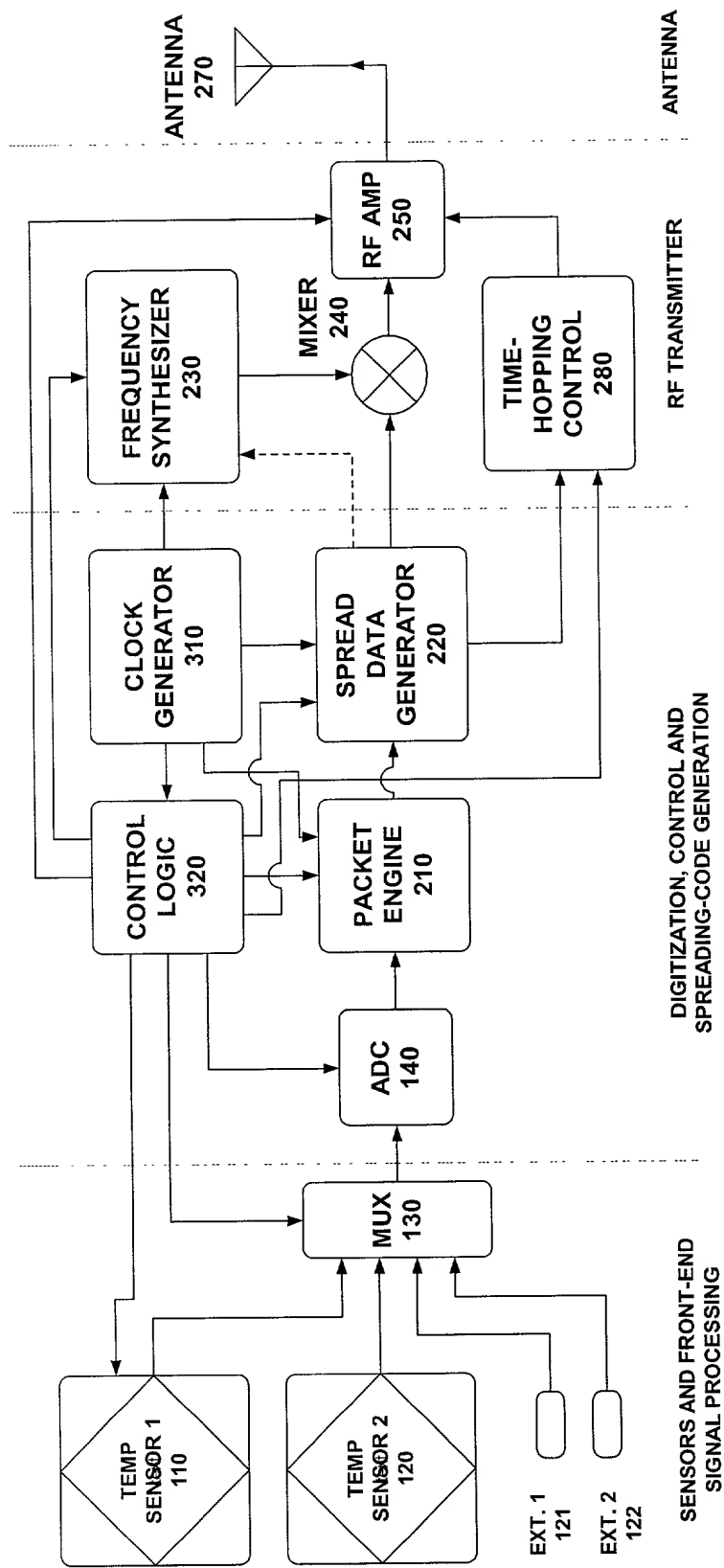


Fig. 8

ORNL Wireless Temperature Telesensor Chip

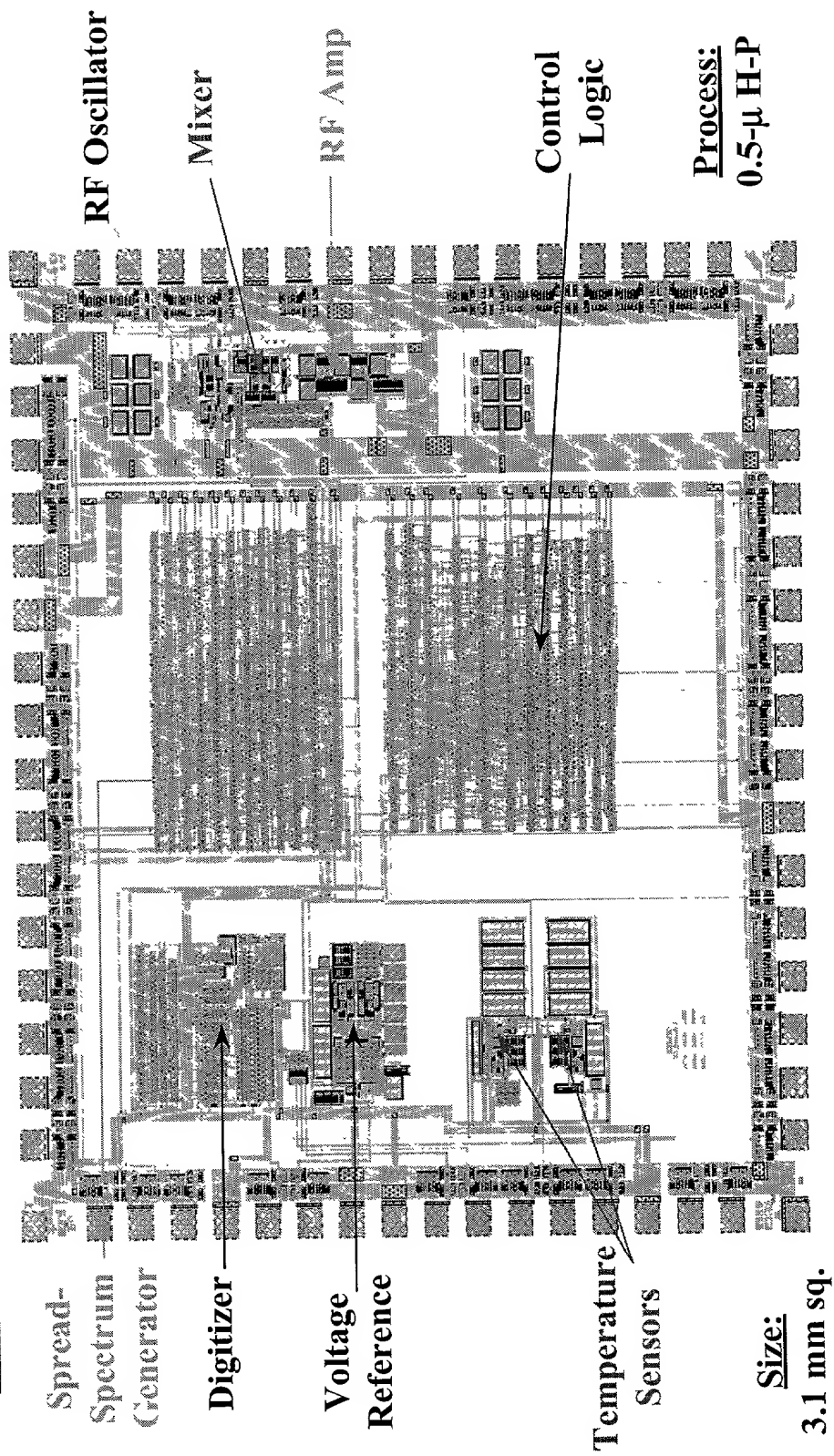


Fig. 9

Advanced Wireless Telesensor Chip

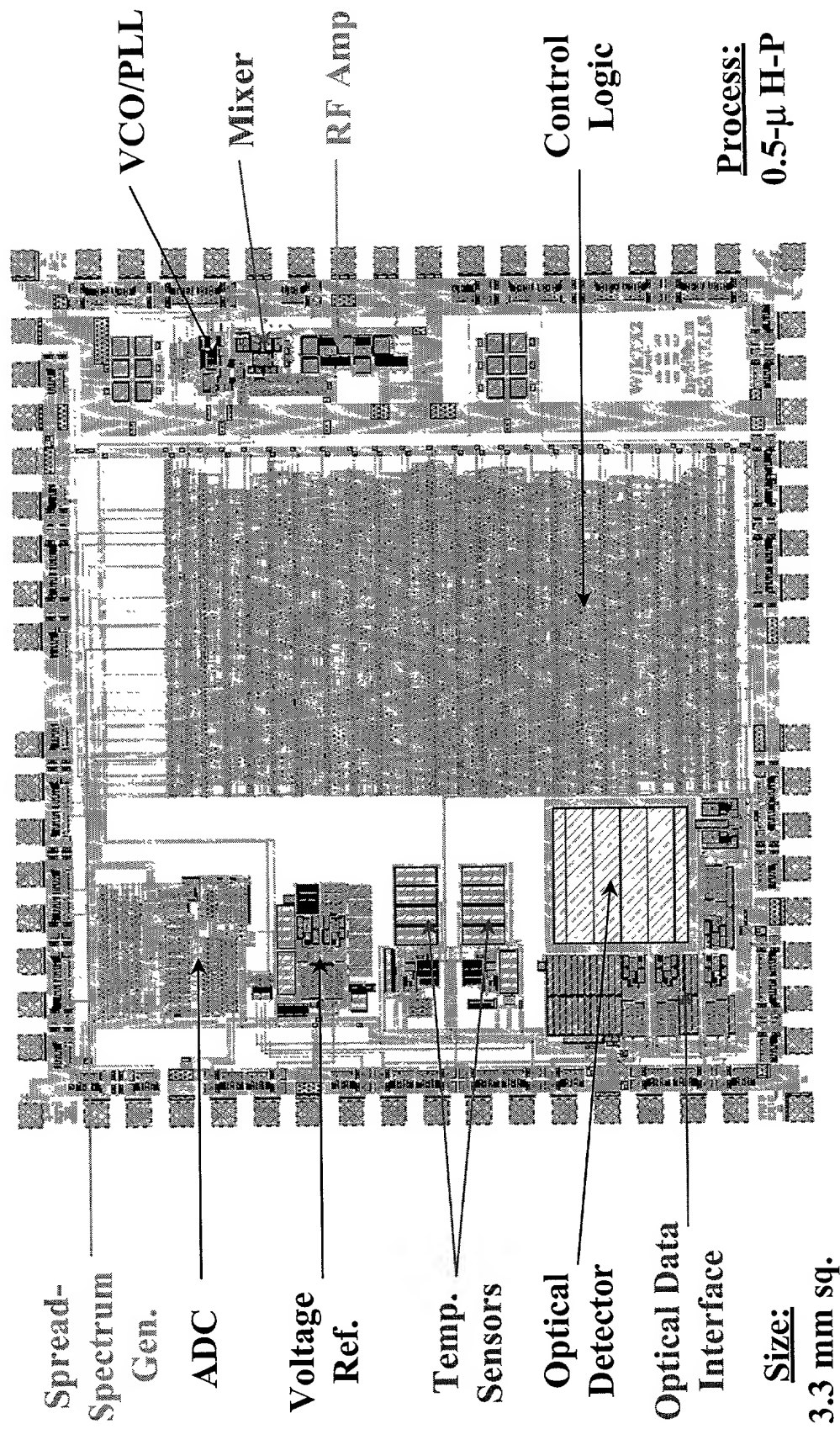


Fig. 10